Sub C e 7

13. (once amended) The power tester of claim 12 further comprising a first connector and a second connector that are linked from the circuitry to two separate devices, the first connector configured for the voltage disturbances that are due to an increase in voltage and the second connector configured for the voltage disturbances that are due to a decrease in voltage.

REMARKS

The Applicant has carefully read and reviewed the Office Action mailed July 11, 2002, and the references cited therewith. Claims 1-17 were rejected. Claims 4, 5, 6, 8, and 13 have been amended. Claims 1-17, as amended, are now pending in the application. A corrected information disclosure statement is being filed with this response, as requested per the Examiner.

Rejections under 35 U.S.C. § 112

Claims 4, 8, and 13 were rejected under 35 U.S.C. § 112, 2nd paragraph as being indefinite. The Applicant thanks the Examiner for the suggested wording to better define the claims. The Applicant believes the amendments to Claims 4, 8, and 13 should suffice to overcome the rejections. Claims 5 and 6 were similarly amended to clear up any possible confusion in the claims.

Rejections under 35 U.S.C. § 102

Claims 1-3, 8-10 and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Arnoldi (US 3,979,672). Arnoldi describes a system for testing only a transistor under test (TUT) by increasing the collector current level. Arnoldi does not disclose applying a nominal voltage, introducing a voltage disruption, and repeating the voltage disruption.

Specifically, Arnoldi does not describe introducing a voltage disruption. Instead Arnoldi incrementally changes a voltage so as to control the increases made to a transistor collector current. To do this,

Arnoldi discloses using a ramp generator to increment a voltage that is then used to control the collector current. Arnoldi's purpose of using a voltage ramp generator shows the inherent and distinct differences between Arnoldi and the present invention. **Arnoldi uses a voltage ramp generator specifically so that the TUT is not subjected to a large current increase due to a voltage disruption.** (Arnoldi, Col. 3, Lines 2-8)

Further, the present application describes a voltage disruption as being a voltage spike or a low voltage condition. Arnoldi's design for monitoring a collector current does not describe, discuss, or even suggest that the TUT be subjected to a voltage disruption, as described in the present description and claims. As stated previously, Arnoldi's use of a ramp generator evidences the design choice not to subject the TUT to a high or low voltage condition; hence, Arnoldi does not provide a voltage disruption as defined by the present application.

Yet even further, if we ignore the fact that Arnoldi does not even disclose a voltage disruption, **Arnoldi does not describe repeating a voltage disruption either**, as described in the amended claims. Arnoldi's design states that once the increments in current has caused secondary breakdown, the test is terminated. The test is not repeated. (Col. 2, L. 53-58) This is due to the fact that Arnoldi's design is testing for the safe operating level of the collector current; thus, Arnoldi is not testing for unexpected power disruptions. Arnoldi does not teach or suggest the use of repeated voltage disruptions to test a component, all of which is described in the present independent claims.

For a prior art to anticipate under 35 U.S.C. § 102(b), the prior art has to meet every element of the claimed invention. It is clear that Claims 1-3, 8-10 and 17 all of which describe repeating voltage disruptions are distinguishable from the designs suggested in Arnoldi (US 3,979,672).

In summary, the present claims have significant distinguishable features over Arnoldi (US 3,979,672). Therefore, the rejection of claims 1-3, 8-10, and 17 under 35 U.S.C. § 102(b) should be withdrawn.

The Examiner is respectfully reminded that claim 17 is written in means-plus-function form and therefore deserves the analysis accorded to it by the USPTO as promulgated under the supplemental guidelines for the examination of claims written in accordance with 35 U.S.C. §112, ¶6. These guidelines are applicable to and guide the determination of the patentability of the claims in the present case. See *Supplemental Examination Guidelines for Determining the Applicability of 35 U.S.C. 112, P6*, 65 FR 38510, Federal Register Vol. 65, No. 120, June 21, 2000.

Rejections under 35 U.S.C. § 103

Claims 4-7 and 11-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable. Applicant respectfully traverses the rejection of claims 4-7 and 11-16. Claims 4-7 and 11-16 are dependent claims which ultimately depend from claim 1 or claim 8, both of which are believed to be patentable over the prior art of record for the reasons discussed hereinabove. Claims 4-7 and 11-16 are thus allowable as dependent claims depending from allowable independent claims and providing additional limitations thereto. Reconsideration and withdrawal of the rejection of claims 4-7 and 11-16 is respectfully requested.

Conclusion

For the aforementioned reasons, claims 1-17 are believed to be patentable over the prior art of record, therefore, reconsideration and withdrawal of the rejection of claims 1-17 is requested. Applicant respectfully asserts that the present claims particularly point out and distinctly claim the subject matter which is regarded as the invention.

Therefore, it is respectfully submitted that the pending claims are in condition for allowance, and favorable action with respect to the present application is requested.

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MARKED UP VERSION OF AMENDED ABSTRACT

(The 2 paragraphs were combined.)

COMPREHENSIVE APPLICATION POWER TESTER

Abstract of the Disclosure

An electronic device power testing method is provided in which applying a nominal voltage to an electronic component, introducing a voltage disruption to the nominal voltage, and repeating the voltage disruption for a specified number of instances is done. The present invention also can be implemented as an electronic device power tester.

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MARKED UP VERSION OF AMENDED CLAIMS

4. (once amended) The method of claim 1 further comprising ~~wherein step (d), prior to step (a), comprises~~ applying a sequence of voltages during power-on, wherein a second voltage is activated a specific amount of time after a first voltage was activated.

5. (once amended) The method of claim 1 further comprising ~~wherein step (d) comprises~~ applying a sequence of voltages during power-off, wherein a second voltage is deactivated a specific amount of time after a first voltage was deactivated.

6. (once amended) The method of claim 1 ~~wherein step (d), prior to step (b), comprises~~ further comprising adjusting a combination of variables selected from the group consisting of voltage disruption frequency, voltage disruption time duration and voltage disruption magnitude.

8. (once amended) An electronic device power tester, comprising:

(a) at least one power source;

(b) circuitry coupled to ~~a~~ the at least one power source, the circuitry being configured to produce a voltage disturbance and repeat the voltage disturbance for a specified number of instances; and

(c) a connector linked from the circuitry to a device.

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13. (once amended) The power tester of claim 12 ~~wherein there are two connectors~~ further comprising a first connector and a second connector that are linked from the circuitry to two separate devices, ~~one~~ the first connector configured for the voltage disturbances that are due to an increase in voltage and the ~~other~~ second connector configured for the voltage disturbances that are due to a decrease in voltage.